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UNITED STATES DISTRICT COURT
NORTHERN DISTRICT OF CALIFORNIA
SAN JOSE DIVISION

VLSI TECHNOLOGY, LLC,

Plaintiff,

v.

INTEL CORPORATION,

Defendant.

Case No. 5:17-cv-05671-BLF-NC

INTEL CORPORATION'S MEMORANDUM OF POINTS AND AUTHORITIES IN SUPPORT OF ITS OMNIBUS MOTION FOR SUMMARY JUDGMENT

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Exhibits

The exhibits cited in the motion as "Ex. __" are attached to the Declaration of Mark Selwyn filed herewith.

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I. INTRODUCTION

Intel respectfully requests summary judgment (1) of no infringement for the four asserted patents, U.S. Patent Nos. 8,566,836 ("'836 patent"), 8,004,922 ("'922 patent"), 7,675,806 ("'806 patent"), and 8,268,672 ("'672 patent"), (2) of invalidity of the asserted claims for the '922 patent, (3) that it is licensed to all asserted patents, and (4) of no willful infringement, no indirect infringement, and no enhanced damages for any patent.

II. LEGAL STANDARD

Summary judgment is appropriate when there "is no genuine dispute as to any material fact and the movant is entitled to judgment as a matter of law." Fed. R. Civ. P. 56(a); *see Anderson v. Liberty Lobby, Inc.*, 477 U.S. 242, 247 (1986). To defeat summary judgment, the nonmoving party must come forward with "specific facts showing that there is a genuine issue for trial." *Matsushita Elec. Indus. Co. v. Zenith Radio Corp.*, 475 U.S. 574, 586-87 (1986) (emphasis omitted).

III. INTEL IS ENTITLED TO SUMMARY JUDGMENT OF NO INFRINGEMENT OF THE '836 PATENT.

VLSI accuses Intel of infringing eight claims of the '836 patent, all of which require a specific sequence of steps, including the need to identify whether a task is a single-core task before selecting or identifying the core on which to run that single-core task. Intel is entitled to summary judgment of no literal infringement because the undisputed record confirms that its accused products never identify whether a task is a single core-task before selecting or identifying the core on which to run the given task. Intel also is entitled to summary judgment under VLSI's doctrine of equivalents ("DOE") theory—which covers selecting a core for a task without first identifying if it is a single-core task—because that theory is barred by both amendment- and argument-based prosecution history estoppel, and also because it would vitiate the claim limitation. Intel is further entitled to summary judgment of no infringement because what VLSI has accused of infringement undisputedly occurs solely outside the United States.

A. Technical Background And Asserted Claims

Computer processors contain circuitry called "cores" that execute a sequence of instructions (which the '836 patent sometimes calls a "task"). A "task" can consist of one or more software

"threads," which are independently executable groups of instructions. A "multicore" processor contains two or more cores. The existence of multiple cores allows the processor to execute multiple tasks in parallel, which can include having different cores run different tasks at the same time, or spreading a single task across multiple cores. Dkt. 1-8 ['836 patent], 1:11-16, 3:64-4:7. The '836 patent refers to "single-core" tasks as tasks that can only run on a single core, and "multicore" tasks as tasks that can run across multiple cores. *Id.* at 1:56-2:13, 6:6-7:11, Fig. 3. Within the same processor, different cores can run at different operating frequencies (speeds). *Id.* at 1:16-20, 2:64-3:3.

VLSI accuses Intel of infringing claims 1, 9-11, 13, 17, 20, and 21. Each asserted claim requires, among other things, that "upon identifying" a task as a single-core task, the fastest core in the processor is "select[ed]" (claims 1, 9-11, 13, 17) or "identified" (claims 20, 21) to run that single-core task. Dkt. 241 [*Markman* Order] 22-25 (construing claim 10 to include same "upon identifying" limitation as claims 1 and 20). In other words, each asserted claim requires identifying a single-core task ***as a predicate*** to selecting or identifying the core on which to run that task. According to the '836 patent, this approach allows the computer's operating system to direct a task to the fastest core when the task cannot be run across multiple cores. '836 patent at 2:1-13.

During claim construction, the Court rejected VLSI's attempt to eliminate the "upon identifying" claim requirement to identify a single-core task as a predicate to selecting the core on which to run that task. As the Court ruled, the applicants "clearly and unmistakably admitted" during prosecution that the claims require identifying a single-core task before selecting the core on which to run that task (to distinguish prior art). Dkt. 241 [*Markman* Order] 22-25.

B. Intel's Accused Products

VLSI accuses Intel processors with features called "Turbo Boost Max Technology 3.0" and "Thread Director" of infringing the '836 asserted claims. Ex. 1 [Conte Rpt.] ¶¶ 131, 135; Ex. 2 [Conte Dep.] 130:10-17. VLSI's technical expert, Dr. Thomas Conte, contends that in the accused Intel products, "the selection step" of the asserted claims "occurs" when the operating system scheduler assigns a "thread" to a core. Ex. 1 [Conte Rpt.] ¶¶ 412-14; Ex. 2 [Conte Dep.] 139:6-23. But it is undisputed this core selection occurs before the accused products ever allegedly identify that the task is a single-core task. Ex. 2 [Conte Dep.] 139:6-23 (Intel's accused products "allow[] the operating

system to select the favored core"); 133:21-134:16 (code in Intel's products that allegedly identifies a single-core task is invoked "[o]nce a thread is scheduled on a core" by the operating system) *id*. at 136:12-22 (code in Intel's accused products allegedly identifies a "single-core task" when it "discovers that there is only one active core running"); Ex. 1 [Conte Rpt.] ¶¶ 416-17. Indeed, every fact witness addressing this issue confirmed the accused products never identify whether a task is a single-core task—let alone before selecting a core for the task. Ex. 3 [Ramani Dep.] 165:5-166:11; Ex. 4 [McGavock Dep.] 110:13-112:21; Ex. 6 [Therien 1/27/23 Dep.] 403:8-18, 405:5-15; Ex. 7 [Chen Dep.] 119:17-120:6; Ex. 8 [L. Brown Dep.] 179:16-180:11, 183:20-184:25; Ex. 9 [Fenger Dep.] 160:1-7, 165:24-167:8; Ex. 10 [T. Brown Dep.] 15:14-16:5, 16:25-17:16, 19:19-20:8.

Apparently recognizing that Intel's products never identify whether tasks are single-core tasks, Dr. Conte instead points to something in the source code that determines how many cores are active at any given time. Ex. 2 [Conte Dep.] 138:2-15; Ex. 1 [Conte Rpt.] ¶¶ 416-17, 427, 433, 439, 448, 454, 460, 466. Dr. Conte contends that when this code determines that only a single core is active, the code is identifying a single-core task as required by the claims. Ex. 2 [Conte Dep.] 138:2-15; Ex. 1 [Conte Rpt.] ¶¶ 416-17, 427, 433, 439, 448, 454, 460, 466. But there is no dispute that the code in Intel's products only determines how many cores are active "[o]nce a thread is scheduled on a core." Ex. 2 [Conte Dep.] 133:21-134:16. In other words, it is undisputed that what Dr. Conte points to in the accused products as identifying a single-core task (i.e., the code determining how many cores are active) occurs ***after*** a core has already been selected or identified. *Id.* at 136:23-139:23 (confirming order of steps in the accused products).

C. Intel Is Entitled To Summary Judgment Of No Literal Infringement.

Summary judgment of no infringement is required under VLSI's literal infringement theory. The plain language of the "upon identifying" limitation specifies that selecting (claims 1, 9-11, 13, 17) or identifying (claims 20, 21) the core to run a single-core task occurs only ***after*** identification of the task as a single-core task (which makes sense in view of the patent's goal to send single-core tasks to the fastest core, which cannot occur unless the system first knows a task is single-core or not). Dkt. 143 [VLSI *Markman* Br.] 20 (agreeing "upon identifying" is "a temporal term that describes ***when*** something happens"); Dkt. 145 [Conte *Markman* Decl.] ¶ 181 (same); Dkt. 158-13 ['836 File History]

1934 (Examiner requiring applicants "to amend independent claims 1, 10, and 20 to clarify that a core is selected from the plurality of cores ***when*** it is identified that a task cannot be run across the plurality of cores" as a condition for allowing the patent to issue).[1] In other words, the "upon identifying" limitation "specifies a predicate" to the selection of a core, as Dr. Conte recently reiterated. Ex. 2 [Conte Dep.] 100:9-11.

Because it is undisputed that cores are selected or identified ***before*** the code performs the operation that Dr. Conte opines is the alleged identification of a single-core task, *e.g.*, Ex. 2 [Conte Dep.] 136:23-139:23, the undisputed facts demonstrate that a core is not identified or selected "upon identifying a single-core task" as required by every asserted claim. Therefore, the Court should grant summary judgment of no literal infringement of any asserted claim of the '836 patent.

D. Intel Is Entitled To Summary Judgment Of No Infringement Under The DOE.

VLSI and Dr. Conte alternatively assert that the "upon identifying" limitation is met under the DOE because Intel's accused products supposedly select a core "substantially simultaneously" with identifying a single-core task. Ex. 1 [Conte Rpt.] ¶¶ 471-72. But that argument fails as a matter of law for multiple reasons.

First, amendment-based prosecution history estoppel forecloses VLSI from alleging any broader scope for this claim limitation under the DOE. During prosecution, claim 20 was narrowed by amendment to add the limitation "upon identifying a processing task that cannot be run across the plurality of the multiple cores." Dkt. 158-13 ['836 File History] 1941. The applicants relied on this claim language during prosecution to distinguish the prior art that disclosed selecting cores for other reasons. *Id.* at 1878 ("[T]he claims require identification of 'a ***processing task*** that can not be run by the plurality of core.' *See, e.g.*, claim 1 ('upon identifying ***a processing task*** that can not be run by the plurality of cores …')[.]"); *id.* at 1906 ("the cited art references fail to disclose or suggest[] identifying tasks 'that cannot be run by the plurality of cores' and assigning such single-core tasks to the fastest core[.]"); *id.* at 1916 ("Bernstein does not distinguish between 'multi-core' applications and 'single core' applications."); *id.* at 1916-1917 ("[T]he cited Bernstein and Ghiasi references fail to

[1] All bold/italics emphasis in this brief is added.

disclose or suggest the claim requirement that 'multi-core' applications and 'single-core' applications are handled separately…."). And the examiner conditioned allowance of the claims on amending claim 20 to include this language to distinguish the prior art. *Id.* at 1934, 1941. Although this amendment was made to claim 20, it is clear from the prosecution history that the amendment was made to align the scope of all claims with respect to the "upon identifying" limitation. *Id.* at 1934 ("It was ***agreed*** to amend independent claims ***1, 10, and 20 to clarify that a core is selected from the plurality of cores when it is identified that a task cannot be run across the plurality of cores***."); *see Old Town Canoe Co. v. Confluence Holdings Corp.*, 448 F.3d 1309, 1314-15 (Fed. Cir. 2006) (amendment-based prosecution history estoppel applies to other non-amended claims containing the same limitation). Amendment-based prosecution history estoppel therefore prohibits VLSI from expanding this limitation through the doctrine of equivalents to cover products that select the fastest core without first identifying a single-core task. *See Festo Corp. v. Shoketsu Kinzoku Kogyo Kabushiki Corp.*, 535 U.S. 722, 736 (2002) ("Estoppel arises when an amendment is made to secure the patent and the amendment narrows the patent's scope.").

Second, argument-based prosecution history estoppel also bars VLSI's equivalents theory. "To invoke argument-based estoppel, 'the prosecution history must evince a clear and unmistakable surrender of subject matter." *Amgen, Inc. v. Coherus BioSciences, Inc.*, 931 F.3d 1154, 1159 (Fed. Cir. 2019). That is exactly what happened here, as the Court found during claim construction, based on the applicants' repeated reliance on the "upon identifying" limitation to distinguish every asserted claim from the prior art during prosecution. Dkt. 241 [*Markman* Order] 24 ("The applicants' statement quoted above is a clear and unmistakable disavowal of a broader interpretation of claim 10 and on its own sufficient to find prosecution disclaimer."); Dkt. 158-13 ['836 File History] 1877 (applicant stating "claims ***1, 10, and 20***" all require ***"upon identifying*** a single-core processing task that cannot be run by the plurality of cores, the core having the fastest measured processing speed parameter is selected to run the identified single-core processing task"); *id.* at 1913-14 (same); *id.* at 1934 ("It was agreed to amend independent claims ***1, 10, and 20*** to clarify that a core is selected from the plurality of cores ***when it is identified that a task cannot be run across the plurality of cores***."). Having successfully used the "upon identifying" limitation to distinguish prior art during prosecution, VLSI

cannot expand that limitation through the DOE to cover products that do not identify a single-core task first before selecting the fastest core. *See Amgen*, 931 F.3d at 1160 (finding argument-based estoppel where applicants "clearly and unmistakably surrendered" broader claim scope through arguments distinguishing prior art during prosecution).

Finally, VLSI's DOE theory also fails as a matter of law because it would vitiate the "upon identifying" limitation—which, as noted above, this Court held is a mandatory requirement of every asserted claim—by allowing the claims to be met if a single-core task is sent to the fastest core for ***any*** reason, including those having nothing to do with whether the task is a single-core task. That is not a permissible application of the DOE. *Freedman Seating Co. v. American Seating Co.*, 420 F.3d 1350, 1359-1362 (Fed. Cir. 2005) (rejecting DOE theory that "render[ed] the pertinent limitation meaningless" because it would permit any structure to satisfy limitation).

* * *

The accused Intel products undisputedly do not follow the claimed sequence of selecting or identifying a core "upon identifying" a single-core task, and VLSI is barred as a matter of law from using the DOE to stretch its claims to cover Intel's different operations. The Court thus should grant summary judgment of no infringement for all asserted claims of the '836 patent.

E. Intel Is Also Entitled To Summary Judgment Of No Infringement For The '836 Patent Because Intel's Testing Occurs Outside The United States.

Claims 1, 9, 20, and 21 recite methods that, among other things, require "measuring" the processing speed of each core in a multicore processor. VLSI alleges that Intel performs the claimed "measuring" step only when Intel tests its products during manufacturing. Ex. 1 [Conte Rpt.] ¶¶ 307-63, 541-45; Ex. 2 [Conte Dep.] 84:8-85:23 (describing Intel's testing). However, it is undisputed that Intel performs this testing exclusively in Costa Rica and Malaysia. Ex. 5 [Therien 1/26/23 Dep.] 181:17-25; Ex. 6 [Therien 1/27/23 Dep.] 399:20-400:9; Ex. 11 [Cavagnaro Dep.] 158:16-159:19, 160:19-161:6; Ex. 12 [Johnson Dep.] 41:23-25. Because a method claim is infringed only if all steps are practiced in the United States, Intel is entitled to summary judgment of no infringement for claims 1, 9, 20, and 21. *NTP, Inc. v. Research In Motion, Ltd.*, 418 F.3d 1282, 1318 (Fed. Cir. 2005) ("[A] process cannot be used 'within' the United States as required by section 271(a) unless each of the steps

is performed within this country."); *France Telecom S.A. v. Marvell Semiconductor Inc.*, 82 F. Supp. 3d 987, 998 (N.D. Cal. 2015) (granting JMOL of no infringement because the patentee "did not produce any evidence that [the defendant] used the claimed method in the United States").

Similarly, claims 10-11, 13, and 17 recite a "system on a chip" that, among other things, contains "a performance measurement circuit ***for measuring a performance parameter value*** for said core." Under Federal Circuit precedent, the claim language "for measuring" requires that the accused products are "reasonably capable" of performing the claimed function. *INVT SPE LLC v. ITC*, 46 F.4th 1361, 1375-76 (Fed. Cir. 2022). Here, VLSI has alleged that the accused products contain circuitry that satisfies this "measuring" limitation. Ex. 1 [Conte Rpt.] ¶ 493. However, it is undisputed that the accused circuitry is only used for measuring values when connected to an external testing device called an "ATE tester" that is part of Intel's manufacturing facilities in Costa Rica and Malaysia. Ex. 11 [Cavagnaro Dep.] 158:16-159:19, 160:19-161:6, 166:16-167:8, 170:2-171:18; Ex. 2 [Conte Dep.] 109:21-110:6; Ex. 1 [Conte Rpt.] ¶ 339 ("Intel uses an ATE tester as part of the test apparatus."). Dr. Conte testified that he had not offered any opinion that the accused circuitry is capable of measuring a performance parameter value apart from when connected to an external tester at Intel's manufacturing facilities overseas. Ex. 2 [Conte Dep.] 111:4-113:18. Because VLSI cannot show that the accused circuitry in Intel's products is capable of "measuring a performance parameter value" in the United States, Intel is entitled to summary judgment of no infringement for claims 10-11, 13, and 17 as well. *INVT*, 46 F.4th at 1377 (finding no infringement where no evidence existed that accused apparatus was capable of performing claimed function).

Lacking evidence that the claimed "measuring" limitations are ever practiced in the United States, VLSI instead relies on the parties' stipulation that allocates an agreed-upon percentage of Intel's global sales, revenues, and profits for the accused products to the United States. Ex. 1 [Conte Rpt.] ¶¶ 86-89 (citing Ex. 13 [U.S. Nexus Stip.] 2 ("Of the total, global number of Intel products and associated activities determined (without regard to geographic considerations) to meet the technical requirements of any asserted VLSI patent claim not proved invalid by Intel, as well as any actual or projected revenues or profits associated therewith, seventy percent (70%) thereof will be deemed to have a United States nexus as required by each subsection of 35 U.S.C. § 271 and for determining any

patent infringement damages in this case.")). However, the stipulation does not make conduct occurring wholly outside the United States infringing; the stipulation expressly states that it is not an admission of infringement. Ex. 13 [U.S. Nexus Stip.] ("By entering into this agreement, neither party makes any admission about patent infringement…."); *id.* ("This agreement does not in any way suggest or indicate that any of the Intel products at issue infringe…."). VLSI may not rely on this stipulation as a substitute for evidence of infringement within the United States.

IV. INTEL IS ENTITLED TO SUMMARY JUDGMENT OF NO INFRINGEMENT OF THE '922 PATENT.

Summary judgment of no infringement should enter for the '922 patent given VLSI's failure to identify anything in Intel's accused products that constitutes converting a "VSS" reference signal—a requirement of each asserted claim. VLSI's attempt to avoid that result via a flawed claim construction argument should be rejected as a matter of law.

VLSI accuses Intel of infringing claims 4, 5, and 18 of the '922 patent. There is no dispute that each of those claims requires a "supply power converter" that converts "***external supply signal (VDD)***," and a "reference power converter" that converts "***reference signal (VSS)***." Dkt. 1-5 ['922 patent], claims 1, 4 (requiring "external supply signal (VDD)" and "a supply power converter … configured to convert a supply voltage of the external supply signal," and "reference signal (VSS)" and a "reference power converter [] configured to convert a reference voltage of the reference signal"); *id.*, claim 5 (includes same requirements as claim 4, from which it depends); *id.*, claims 17, 18 (requiring a "supply power converter" that receives "external supply signal (VDD)," and a "reference power converter [] configured to change at least one power characteristic of a reference signal (VSS)").[2]

VLSI's technical expert Dr. William Mangione-Smith accuses Intel's Fully Integrated Voltage Regulator ("FIVR") as the claimed "supply power converter," and accuses a signal called "VCCIN" (also called "Vcc" or "Vin") as the claimed "external supply signal (VDD)." Dr. Mangione-Smith

[2] During IPR proceedings, the Patent Office canceled independent claims 1 (from which claims 4 and 5 depend) and 17 (from which claim 18 depends). Ex. 14 [Final Written Decision] at 2, 91-92.

further accuses certain components within the same FIVR as the claimed "reference power converter." There is no dispute, however, that Dr. Mangione-Smith has not identified any accused product that converts "VSS," but rather has identified the ***same*** VCCIN signal as meeting ***both*** the "external supply signal (VDD)" and "reference signal (VSS)" limitations. Ex. 15 [Mangione-Smith Suppl. Rpt.] ¶¶ 197-202, 207-16, 227-47; Ex. 16 [Mangione-Smith Dep.] 73:4-77:19, 94:11-95:13, 127:12-134:12.[3] At the same time, Dr. Mangione-Smith admits that VDD and VSS ***cannot*** be the same voltage signal (because VDD is measured relative to VSS). Ex. 16 [Mangione-Smith Dep.] 132:8-134:12, 135:6-11, 136:22-138:3, 172:23-173:6. Nor could he argue VDD and VSS can be the same because the '922 patent describes VDD and VSS as different voltage signals. Dkt. 1-5 ['922 patent], 2:16-30, 2:44-53, 5:63-67, 6:52-53, 8:26-53 ("external supply signal, VDD"); *id.*, 5:10-17, 6:64-65, 7:50-54, 8:26-53 ("reference signal, VSS"); *id.*, Figs. 1-6 (all depicting "VDD" as a separate voltage signal at the header of the power island and "VSS" as the voltage signal at the footer of the power island); *id.*, Fig. 4 (showing VDD as "1.0V" and VSS as "0.0V"); Ex. 20 [Apsel Rebuttal Rpt.] ¶¶ 144-167.

VLSI's failure to identify any component that converts a VSS signal requires summary judgment of no infringement for each asserted claim. *See Johnston v. IVAC Corp.*, 885 F.2d 1574, 1578 (Fed. Cir. 1989) ("[T]he accused infringer … is entitled to summary judgment, on the ground of non-infringement, by pointing out that the patentee failed to put forth evidence to support a finding that a limitation of the asserted claim was met by the structure in the accused devices.").

Because VLSI is not able to identify any component that converts "VSS" as required by the claims, VLSI's infringement case relies on the flawed argument that "VSS" is not a limitation at all, merely because it appears inside parentheses in the claim ("reference signal (VSS)"). Ex. 17 [Mangione-Smith Reply Rpt.] ¶¶ 156-61. The question of infringement is thus one of claim construction amenable to summary judgment. *See General Mills, Inc. v. Hunt-Wesson, Inc.*, 103 F.3d 978, 983 (Fed. Cir. 1997) ("Where the parties do not dispute any relevant facts regarding the accused

[3] VLSI has asserted that the "reference signal (VSS)" limitation is satisfied literally (not under the doctrine of equivalents), and Dr. Mangione-Smith did not offer any opinion on the "reference signal (VSS)" limitation under the doctrine of equivalents. *See* Ex. 16 [Mangione-Smith Dep.] 99:4-101:14.

product, … but disagree over possible claim interpretations, the question of literal infringement collapses into claim construction and is amenable to summary judgment."). VLSI's claim construction should be rejected for the following reasons.

First, "VSS" is an ***express*** claim term recited in asserted claims 4, 5, and 18, and therefore limits the type of "reference signal" to a particular type of signal, "VSS." VLSI's contention that an express term should be given no effect is contrary to established principles of patent law. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) ("It is a 'bedrock principle' of patent law that 'the claims of a patent define the invention to which the patentee is entitled the right to exclude.'); *Intel Corp. v. Qualcomm Inc.*, 21 F.4th 801, 810 (Fed. Cir. 2021) ("It is highly disfavored to construe terms in a way that renders them void, meaningless, or superfluous."); *Bicon, Inc. v. Straumann Co.*, 441 F.3d 945, 950 (Fed. Cir. 2006) ("[C]laims are interpreted with an eye toward giving effect to all terms in the claim.").

Second, the specification confirms that "VSS" is limiting. The stated purpose of the reference power converter is specifically to change "VSS" by a certain amount purportedly to simplify communications within the power island. Dkt. 1-5 ['922 patent], 7:34-49; 7:57-8:7; Figure 4 (showing VSS being raised from 0.0V to 0.2V). And the specification consistently describes using "VSS" as the reference signal—in every single embodiment. *E.g.*, Dkt. 1-5 ['922 patent], 5:10-17, 6:64-65, 7:50-54, 8:26-53 ("reference signal, VSS"); Figs. 1-7 (all describing the "reference signal" as "VSS"); Ex. 20 [Apsel Rebuttal Rpt.] ¶¶ 55-60, 63-67, 144-167. Accordingly, the claim term "VSS"—when read in light of the specification—is a limitation. *Phillips*, 415 F.3d at 1315 ("Claims 'must be read in view of the specification, of which they are a part.'").

Third, VLSI's argument that an express claim limitation has no meaning merely because it appears in parentheses has been rejected by the Federal Circuit. *Janssen Pharmaceutica, N.V. v. Eon Labs Mfg., Inc.*, 134 F. App'x 425, 428 (Fed. Cir. 2005) ("The mere fact that a limitation is placed within parentheses does not mean it is no longer a part of the claim."). In *Janssen*, the Federal Circuit construed the term "(25-30 mesh)" as limiting, even though it appears in parentheses, in part because the specification repeatedly described embodiments using the same range found recited in the claim

term in parentheses. *Id.* Here, just as in *Janssen*, the '922 patent specification repeatedly describes using "VSS" as the reference signal, just as recited in the asserted claims.

Finally, VLSI's argument ignores that claim 5, which depends on claim 4, specifically recites a "VSS switch" as part of the "reference power converter." Dkt. 1-5 ['922 patent], claim 5. Claim 5's "switch" is a "***VSS*** switch" because it switches the "VSS" signal recited in claim 4, further confirming that "VSS" in claim 4 is limiting. Dr. Mangione-Smith admits that the "VSS switch" of claim 5 is part of the "reference power converter" of claim 4, and that the term "VSS" cannot be deleted from claim 5 without changing the meaning of that claim. Ex. 16 [Mangione-Smith Dep.] 142:12-143:3, 144:7-20, 160:3-6.

In sum, because VSS is a limitation of every asserted claim, and there is no dispute the accused products do not convert VSS, Intel is entitled to summary judgment of no infringement.

V. INTEL IS ENTITLED TO SUMMARY JUDGMENT THAT THE '922 ASSERTED CLAIMS ARE INVALID AS INDEFINITE.

VLSI accuses Intel of infringing claims 4, 5, and 18 of the '922 patent, each of which claim a "power island" that meets certain requirements. But the patent fails to provide persons of ordinary skill with information sufficient to determine with reasonable certainty when a component is a "power island" and when it is not. Therefore, Intel is entitled to summary judgment that the '922 asserted claims are invalid as indefinite under 35 U.S.C. § 112. *See Nautilus, Inc. v. Biosig Instruments, Inc.*, 572 U.S. 898, 901 (2014) ("[A] patent is invalid for indefiniteness if its claims, read in light of the specification delineating the patent, and the prosecution history, fail to inform, with reasonable certainty, those skilled in the art about the scope of the invention.").

Specifically, the '922 specification describes a "power island" as a group of "components with ***similar*** power requirements":

> One power management design approach ***combines components with similar power requirements into groups, which are referred to as power islands*** or, in some instances, voltage islands. ***All of the components within a power island typically have similar power characteristics*** that are unique from the power characteristics of other power islands.

Dkt. 1-5 ['922 patent] 1:29-35. Thus, the specification suggests that the existence of a "power island" turns on the ***degree of similarity*** between the "power characteristics" of components—without providing any information about how to determine when a component is sufficiently "similar" in that respect to qualify as a "power island."

At the same time, the claims compound that ambiguity by imposing another degree-based standard, but in the ***opposite*** direction—by requiring certain components within the "power island" to have "power characteristics" that are "***different***" (claim 1, from which claims 4 and 5 depend) or "***partially different***" (claim 17, from which claim 18 depends) from the "power characteristics" of other components within the "power island." *Id.*, claim 1 (claiming a "power island comprising" a "hardware device" and "scalable logic" wherein the scalable logic operates at "second power characteristics … different from the first power characteristics of the hardware device"), claim 17 ("second power characteristics" must be "at least partially different from the first power characteristics"). Like the specification, these claims do not provide any metrics or other objective boundaries that persons of ordinary skill can use to determine with reasonable certainty when "power characteristics" are "different" and "partially different"—yet at the same time sufficiently "similar"—to be within the claimed "power island."

This renders the asserted claims invalid as indefinite as a matter of law. *See Varian Med. Sys., Inc. v. ViewRay, Inc.*, No. 19-cv-05697-SI, 2020 WL 4260714, at *6-7 (N.D. Cal. July 24, 2020) (claim for medical device requiring "substantially the same" and "different" cross sections found indefinite where "the specification does not contain objective guidance to inform a POSITA regarding what cross sections would qualify as 'substantially same' or 'different'"); *ACQIS LLC v. Alcatel-Lucent USA Inc.*, No. 6:13-cv-638, 2015 WL 1737853, at *10 (E.D. Tex. Apr. 13, 2015) ("similar in design" in computer system patent was indefinite where plaintiff "was unable to articulate any point at which components or circuitry would cease to be 'similar'" and "the claims fail[ed] to 'provide objective boundaries for those of skill in the art'"); *see also Power Integrations, Inc. v. ON Semiconductor Corp.*, No. 16-cv-06371-BLF, 2018 WL 5603631, at *20 (N.D. Cal. Oct. 26, 2018) ("moderate power level" in power supply circuit patent was indefinite where specification failed to "provide some meaningful way to determine what the moderate value is").

Nor could the first-named inventor, David Evoy, identify objective boundaries for the term "power island." He actually confirmed none exists. As he testified, the meaning of "power island" may be "a quite fluid definition," Ex. 18 [Evoy Dep.] 96:4-17, "could change depending on the context of a meeting and who was there," *id.* at 97:23-98:1, and "might even depend [on] who is sitting across the table from me," *id.* at 96:14-17. So boundless was the term to him that he could not say whether "[w]ithin the context of power management, maybe Manhattan could be a power island." *Id.* at 82:22-24; *see also Media Rights Techs., Inc. v. Capital One Fin. Corp.*, 800 F.3d 1366, 1371 (Fed. Cir. 2015) ("[A] claim is indefinite if its language 'might mean several different things and no informed and confident choice is available among the contending definitions.'").

Accordingly, the '922 asserted claims should be found indefinite as a matter of law.

VI. INTEL IS ENTITLED TO SUMMARY JUDGMENT OF NO INFRINGEMENT OF THE '806 PATENT.

VLSI accuses Intel of infringing four claims of the '806 patent, all of which require a "second mode of operation" in which, under the Court's construction, "both the voltage provided to the first memory and the voltage provided to the second memory ***must be lower than the minimum operating voltage of the first memory***." Dkt. 241 [*Markman* Order] 7. As detailed below, however, VLSI has failed to identify ***any*** "minimum operating voltage" for the memory in Intel's products accused as the claimed "first memory," and therefore Intel is entitled to summary judgment of no infringement.

A. The Asserted Claims

For the '806 patent, VLSI has accused Intel of infringing claim 11, as well as claims 12, 13, and 15 that depend from claim 11. Claim 11 requires a "first memory" and a "second memory," and two different modes of operation: "a first mode of operation" and "a second mode of operation." The Court construed "second mode of operation" to require that, "when in the second mode of operation, both the voltage provided to the first memory and the voltage provided to the second memory ***must be lower than the minimum operating voltage of the first memory***." Dkt. 241 [*Markman* Order] 7. Thus, to prove infringement, VLSI must identify some "minimum operating voltage of the first memory" (and then show the voltage provided to both memories is lower than that minimum operating voltage).

B. Intel's Accused Products

VLSI's expert Dr. Thomas Conte asserts that the "first memory" claim requirement is met by a memory array in Intel's accused products called the "data array." Ex. 19 [Conte Reply Rpt.] ¶ 663. But Dr. Conte fails to identify ***any*** minimum operating voltage for that identified data array memory, as the Court's "second mode of operation" construction requires.

Instead of identifying any minimum operating voltages for the accused data array memory, he asserts that the data array memory consists of numerous individual "bitcells" (or "memory cells") (each of which holds one bit of data), and each individual bitcell has a minimum operating voltage. Ex. 1 [Conte Rpt.] ¶¶ 63, 66-67; *id.* ¶¶ 943-44 (for "second mode of operation" limitation, only comparing purported supply voltages to purported minimum operating voltages of ***bitcells***, not the memory arrays); Ex. 19 [Conte Reply Rpt.] ¶¶ 695, 697, 699, 720, 710-11, 733 (alleging minimum operating voltages only for bitcells, and not data array memory); Ex. 2 [Conte Dep.] 229:8-22 (admitting he was "looking at the minimum operating voltage of the memory ***cell*** topologies" in his report and "did not compare the minimum operating voltage of the memory cell ***arrays***"). Dr. Conte does not allege that the purported minimum operating voltage of a bitcell is the same as the minimum operating voltage of the ***data array memory***; instead, he concedes that the data array memory can operate at voltages "even below" the bitcells' minimum operating voltage. Ex. 19 [Conte Reply Rpt.] ¶ 758; *see also* Ex. 2 [Conte Dep.] 224:15-18 ("[T]he array can have a different, slightly different minimum operating voltage from the first memory cell topology or the second memory cell topology of the memory cells."). And Intel's expert, Dr. Alyssa Apsel, agrees. Ex. 20 [Apsel Rebuttal Rpt.] ¶¶ 267, 443; *see also id.* ¶¶ 403-450.

VLSI has offered no DOE theory for the "second mode of operation." Ex. 2 [Conte Dep.] 215:11-14.

C. Intel Is Entitled To Summary Judgment Of No Infringement.

VLSI is required to show that Intel's products meet the "second mode of operation" limitation literally. Under the Court's claim construction ruling, VLSI cannot do so without (1) identifying the minimum operating voltage of the data array memory that it accuses as the "first memory" and (2) demonstrating that the minimum operating voltage of the data array memory is higher than the voltage

provided to both the first memory and second memory when in the second mode of operation. Dkt. 241 [*Markman* Order] 7 ("[W]hen in the second mode of operation, both the voltage provided to the first memory and the voltage provided to the second memory ***must be lower than the minimum operating voltage of the first memory***."). Here, VLSI and Dr. Conte have failed to identify ***any*** "minimum operating voltage" for the data array memory in Intel's products accused as the claimed "first memory." As a result, Intel is entitled to summary judgment of no infringement for the '806 patent.

Nor can VLSI avoid that result based on Dr. Conte's opinion that a minimum operating voltage exists for each of the numerous individual ***bitcells*** within the accused data array memory. Dr. Conte agrees that the Court's "second mode of operation" construction is directed to the voltage levels of "the memory ***arrays***":

> [T]he claim construction says, which includes a requirement of Claim 11 that, when the second mode of operation of the voltage is supplied to the first and second memory, respectively, must be lower than the minimum necessary for the first mode of operation. ***That is referring to the voltages applied to the arrays***.

Ex. 2 [Conte Dep.] 224:19-225:10. Dr. Conte also admits that the purported minimum operating voltage of a specific bitcell cannot be used as a proxy for the minimum operating voltage of the data array memory itself—because the two can differ, and the data memory arrays can operate at voltages "even below" the bitcells' minimum operating voltage. Ex. 19 [Conte Reply Rpt.] ¶ 758; *see also* Ex. 2 [Conte Dep.] 224:15-18.

VII. INTEL IS ENTITLED TO SUMMARY JUDGMENT OF NO INFRINGEMENT OF THE '672 PATENT.

The sole asserted claim of the '672 patent is directed to a chip-assembly process that includes a step whereby a "solder composition is ***provided as a fluid layer*** on the underbump metallization, which layer ***makes a contact angle of less than 90°*** with the underbump metallization." Summary judgment of no infringement should enter for that claim because there is no genuine dispute of material fact that (1) in Intel's current accused process, solder is "***provided***" ***as a solid*** (not "a fluid layer"), and (2) in an accused, but discontinued process, the contact angle between the solder composition and the

accused underbump metallization was ***not*** "***less than 90***°."

A. The Asserted Claim And Intel's Accused Processes

Asserted claim 2 (which depends from claim 1) is directed to "[a] method of assembly of a first chip to a second chip" that includes a series of steps, including (1) "providing … a solder composition" to "a plurality of bond pads at a surface of the first chip … with an underbump metallization," "wherein the solder composition is provided as a fluid layer on the underbump metallization," and (2) further requiring that the solder composition "makes a contact angle[4] of less than 90° with the underbump metallization." Dkt. 1-7 ['672 patent], claims 1, 2; Dkt. 241 [*Markman* Order] 19 (describing "stack" formed by bond pad, underbump metallization, and solder). The specification explains that a fluid form of solder is "preferably applied" using "immersion soldering" (e.g., by immersion in "a bath" of molten solder). Dkt. 1-7 ['672 patent], 3:23-25, 3:57-61, 4:62-63, 5:12-15, 5:19-21, 6:42-43.

VLSI accuses two Intel assembly processes, the relevant steps of which are undisputed: (1) a current process [redacted] what VLSI accused as the claimed "underbump metallization"; and (2) a discontinued process [redacted] the accused underbump metallization. Ex. 22 [Neikirk Rpt.] ¶¶ 140, 148-49, 153.

B. Intel Is Entitled To Summary Judgment Of No Infringement.

Intel is entitled to summary judgment that it does not infringe the '672 patent because the undisputed facts confirm that neither accused process meets every limitation of claim 2.[5]

Intel's current accused process: As noted above, claim 2 requires a "solder composition provided as a fluid layer." But VLSI's expert, Dr. Dean Neikirk, admits that Intel's current process uses an [redacted], and that he is not accusing [redacted] as "provid[ing] solder as a fluid layer." Ex. 23 [Neikirk Dep.] 151:3-152:3. Thus, because

[4] There is no dispute that the "contact angle" between a liquid and a solid surface can measure the extent to which the liquid "wets"—or spreads over—the surface. Ex. 22 [Neikirk Rpt.] ¶ 250.

[5] VLSI asserts only literal infringement of the '672 patent.

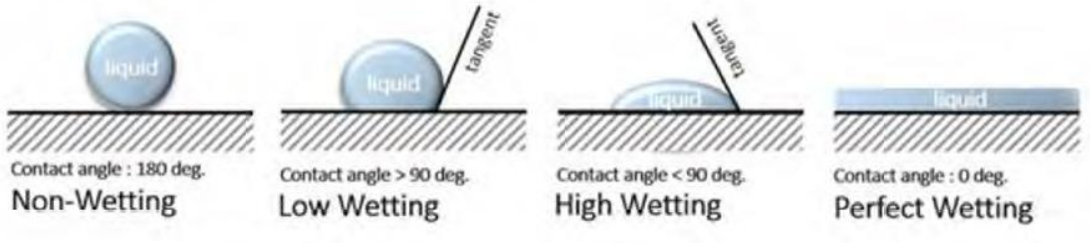
claim 2 requires that the solder composition be "provided ***as a fluid layer***," and because it is undisputed that Intel's current process instead [redacted], Intel is entitled to summary judgment of no infringement for this process.

VLSI alleges that the "provided as a fluid layer" requirement is still met because [redacted]. Ex. 22 [Neikirk Rpt.] ¶ 247. But the plain and ordinary language of claim 2 specifies that the solder must be a fluid ***when applied*** to the underbump metallization ("the solder composition is provided as a fluid layer on the underbump metallization"), and the undisputed facts show that the [redacted]. As a matter of law, VLSI cannot meet that claim requirement simply by arguing that [redacted]. *Id*. ¶¶ 140-41, 247. Indeed, Dr. Neikirk admits that the '672 patent does not describe any embodiment in which [redacted], as a "solder composition provided as a fluid layer on the underbump metallization." Ex. 23 [Neikirk Dep.] 145:22-147:2. Nor does any '672 claim include such a transformation step.

VLSI alternatively asserts that solder "is provided as a fluid layer" [redacted]. Ex. 22 [Neikirk Rpt.] ¶¶ 204, 237. However, that argument fails for the same reasons—because there is no dispute that the [redacted] legally irrelevant for purposes of this limitation. Ex. 23 [Neikirk Dep.] 151:3-152:3.

Intel's discontinued accused process: Even accepting for purposes of this motion VLSI's incorrect theory that Intel's now-discontinued process provided solder paste "as a fluid layer," Intel is entitled to summary judgment of no infringement because VLSI has no evidence that [redacted], as required by claim 2. In fact, VLSI has not identified ***any*** measurement of ***any*** contact angle in ***any*** Intel accused product. Dr. Neikirk instead merely cites to documents regarding [redacted], without any analysis. Ex. 22 [Neikirk Rpt.] ¶ 253. But those documents do not refer to any "contact angle"

between [redacted], let alone one of "less than 90°." Dr. Neikirk attempts to overcome this lack of evidence based on (1) statements that [redacted], and (2) his assertion that a "scientific principle" exists that [redacted] Ex. 22 [Neikirk Rpt.] ¶ 249-250. This conclusory assertion is insufficient to avoid summary judgment—particularly when coupled with the fact that, as shown below, the source Dr. Neikirk cites for this alleged "scientific principle" shows that "wetting" also occur at angles ***between 90° and 180°***, thus undermining his claim that, as a matter of "scientific principle," the angle will always be less than 90°:



Ex. 22 [Neikirk Rpt.] ¶ 250. *See Alpek Polyester, S.A. de C.V. v. Polymetrix AG*, No. 21-1706, 2021 WL 5974163, at *6 (Fed. Cir. Dec. 16, 2021) (holding "no genuine dispute of material fact" sufficient to preclude summary judgment where patentee relied on a "conclusory assertion by its expert" that was "nonsensical in view of" countervailing evidence); *Moore USA, Inc. v. Standard Register Co.*, 229 F.3d 1091, 1112 (Fed. Cir. 2000) (finding allegations in plaintiff's declaration that was "entirely lacking in factual support" insufficient to avoid summary judgment because "[a] party may not overcome a grant of summary judgment by merely offering conclusory statements.").

Given that claim 2 requires "a contact angle of less than 90°" and that Dr. Neikirk's claimed "scientific principle" is conclusory and unsupported by his own citation, Intel is entitled to summary judgment of no infringement for its discontinued process as well.

VIII. INTEL IS ENTITLED TO SUMMARY JUDGMENT OF NO INFRINGEMENT FOR ALL ASSERTED PATENTS BECAUSE INTEL IS LICENSED.

Fortress Investment Group ("Fortress"), the company that formed and controls VLSI, acquired control of Finjan Holdings LLC ("FHL") in 2020. That acquisition triggered Intel's rights under a

2012 Patent License Agreement ("License") to practice patents owned by two FHL subsidiaries ("Finjan Parties") and their "Affiliates." Ex. 24 [License] § 1.2. Because VLSI is an "Affiliate" under the License's plain terms, Intel is licensed to practice VLSI's asserted patents.

Under the License, Intel received a "perpetual, irrevocable license" to "Finjan's Patents," Ex. 24 [License] § 3.1, a term broadly defined to encompass all patent rights "owned or controlled" by "Finjan" within the "Capture Period." *Id*. § 1.10. Notably, the term "Finjan" expressly includes Finjan, Inc., Finjan Software, Inc., ***and their "Affiliates."*** *Id.*, Preamble. "Affiliates" is defined as "any Person that, now ***or hereafter***, directly or ***indirectly*** through one or more entities, controls or is controlled by, or ***is under common control with***, [a] specified Person." *Id*. §1.2.

VLSI and the Finjan Parties are both "Affiliates" under the common control of Fortress. Fortress, which formed VLSI in 2016 to purchase patents from NXP Semiconductors ("NXP"), directed and led the negotiations for VLSI's patent purchase from NXP, Ex. 25 [VLSI Technology Marking Report] at FORTRESS-18-966DE00000913, 915; Ex. 26 [Fortress Investment Overview re: NXP Patent Portfolio] at FORTRESS00051713; Ex. 27 [Slan Dep.] 46:2-16, 54:2-16, 54:23-55:4, 85:20-86:5; Ex. 28 [Shah Dep.] 72:16-73:19, and continues to exercise control over VLSI in multiple ways, including: (1) Fortress installed VLSI's board of directors and still assigns its members, two out of three of whom have always been Fortress employees, Ex. 27 [Slan Dep.] 113:4-15; Ex. 29 [Zur Dep.] 30:13-18, 69:18-70:5, 124:8-125:8; Ex. 28 [Shah Dep.] 50:6-10; and (2) Fortress implemented an independent CFO function that oversees VLSI's expenses and maintains direct access to VLSI's bank account which contains only limited operational funds, Ex. 30 [M. Furstein Email] at FORTRESS00050754-55; Ex. 27 [Slan Dep.] 121:15-123:10; Ex. 31 [S. Brogden Email] at FORTRESS-18-966DEC00000944; Ex. 32 [Brogden Dep.] 41:5-21, 117:16-23; Ex. 33 [VLSI Financial Statements] at FORTRESS00000619, 621. Fortress also controls FHL. Fortress created and controls FHL's parent company; since 2020, Fortress employees have always constituted a majority of FHL's board; and FHL must request funding through Fortress. Ex. 34 [Anderson Dep.] 43:6-13, 43:21-44:12, 45:18-22, 47:15-48:6, 51:14-52:13, 94:17-95:8; Ex. 35 [Schedule Tender Offer Form for Acquiring Finjan Holdings Inc.] at 3, 8, 71-74; Ex. 36 [Hartstein Dep.] 73:20-24, 82:10-20; Ex. 37 [FHL LLC Agreement] at FIN0002453-54, FIN0002457-58.

Although Fortress and VLSI were not Affiliates of the Finjan Parties when the License was signed in 2012, courts applying Delaware law, which governs the License, have held that provisions directed to "affiliates" bind future affiliates. *See, e.g.*, *In re Shorenstein Hays-Nederlander Theatres LLC Appeals*, 213 A.3d 39, 57 (Del. 2019) (affirming "[c]ontracts may impose obligations on affiliates" under Delaware law, and holding that "Affiliate" provisions in 2000 agreement bound non-signatory affiliates, including entity acquired in 2010). The same rule has been applied in patent cases. *E.g.*, *MicroStrategy Inc. v. Acacia Research Corp.*, No. 5735-VCP, 2010 WL 5550455, at *12 (Del. Ch. Dec. 30, 2010) (affiliate formed after a contract's effective date bound "to the same extent" as the contract's signatory under a definition of "affiliate" similar to the one here); *Oyster Optics, LLC v. Infinera Corp.*, 843 F. App'x 298, 300-02 (Fed. Cir. 2021) (under forward-looking definition of "Affiliates," patent license extended to a company that became an affiliate after the license was signed). The Finjan Parties also represented that [redacted] Ex. 24 [License] §§ 8.1, 8.3.

Fortress and VLSI are also bound by the License under Delaware law because they implicitly adopted it. *Am. Legacy Found. v. Lorillard Tobacco Co.*, 831 A.2d 335, 343-344 (Del. Ch. 2003) ("Third parties to an agreement may become parties to it, and thus bound by it, by either expressly or implicitly adopting the agreement."), *aff'd*, 903 A.2d 728, 745 (Del. 2006). Here, (1) Fortress did due diligence on the License before the FHL acquisition; (2) Fortress made itself an affiliate of FHL through the acquisition; and (3) the License confers benefits on Fortress as an affiliate. Ex. 24 [License] § 2.5; Ex. 36 [Hartstein Dep.] 49:20-50:14, 50:24-54:9, 69:6-12, 86:5-14; Ex. 34 [Anderson Dep.] 23:5-13, 24:2-21, 31:9-32:12, 32:23-33:11; Ex. 38 [Finjan Holdings, Inc. Schedule 14D-9] at FIN0003859-60. Fortress thus implicitly adopted the License, thereby binding itself and its affiliates, including VLSI.

VLSI cannot defend against summary judgment based on Judge Albright's ruling in the Western District of Texas that Intel's defense was "futile." That ruling, which is currently on appeal and directly conflicts with an earlier District of Delaware ruling, does not trigger issue preclusion because it rested primarily on alleged procedural default unique to the Texas litigation. *See VLSI Tech. LLC v. Intel Corp.*, 6:21-cv-57, Dkt. 694 at 4, 7 (W.D. Tex. Mar. 18, 2022); *see also* Restatement

(Second) of Judgments § 27, Comment i, at 259 ("If a judgment of a court of first instance is based on determinations of two issues, either of which standing independently would be sufficient to support the result, the judgment is not conclusive with respect to either issue standing alone."); *Comair Rotron, Inc. v. Nippon Densan Corp.*, 49 F.3d 1535, 1538 (Fed. Cir. 1995) ("[W]hen a judgment may have been based on alternative grounds, any of which would be sufficient to support the result, the judgment is not preclusive with respect to any ground standing alone."). Judge Albright also never addressed all the issues before this Court, including the issue of implicit adoption.

IX. INTEL IS ENTITLED TO SUMMARY JUDGMENT OF NO WILLFUL INFRINGEMENT, NO INDIRECT INFRINGEMENT, AND NO ENHANCED DAMAGES.

Summary judgment of no willful infringement, no indirect infringement, and no enhanced damages should enter for the asserted patents because there is no genuine dispute of material fact that Intel was unaware of the patents-in-suit before this case was filed and lacks the requisite "knowledge of infringement."

A. The Court Should Grant Summary Judgment Of No Indirect Infringement And No Willful Infringement.

Indirect and willful infringement both require VLSI to prove, for each asserted patent, that Intel knew or should have known (1) of the patent, and (2) that it was infringing the patent. *See Commil USA, LLC v. Cisco Sys., Inc.*, 575 U.S. 632, 639 (2015) (indirect infringement "requires knowledge of the patent in suit and knowledge of patent infringement"); *Arctic Cat Inc. v. Bombardier Recreational Prods. Inc.*, 876 F.3d 1350, 1371 (Fed. Cir. 2017) (same for willful infringement); *Sonos, Inc. v. Google LLC*, 591 F. Supp. 3d 638, 647 (N.D. Cal. 2022) ("Like willful infringement, both forms of indirect infringement—induced and contributory infringement—require knowledge of the patent and knowledge of infringement.").

First, there is no genuine dispute of material fact that Intel lacked sufficient knowledge of the asserted patents. For three of the asserted patents (the '806, '922, and '672 patents), VLSI failed even to ***allege*** pre-suit knowledge by Intel in its complaint, interrogatory responses, or contentions. Dkt. 1 [Compl.] ¶¶ 47-49, 92-94, 120-22; Ex. 39 [Interrog. Resp.] 8-10 (no mention of '806, '922, and '672

patents regarding knowledge); Dkt. 407-2 [VLSI's Second Amend. Infringement Contentions] 15-17 (same); Dkt. 477-3 [VLSI's Fifth Suppl. Damages Contentions] 216-218 (same). And for the '836 patent, VLSI only has alleged pre-suit knowledge because "a patent examiner cited the application that led to the '836 patent" during prosecution of two other patents, Ex. 39 [Interrog. Resp.] 10—an allegation that multiple courts, including in this District, have found legally insufficient to show the requisite level of knowledge. *See Dali Wireless, Inc. v. Corning Optical Commc'ns LLC*, No. 20-cv-06469-EMC, 2022 WL 16701926, at *5 (N.D. Cal. Nov. 3, 2022) ("Given the breadth of the patents cited in the patent prosecution histories of 75 patents, the scant citation alone to the patents-in-suit do not establish specific knowledge of such patents."); *Spherix Inc. v. Juniper Networks, Inc.*, No. 14-578-SLR, 2015 WL 1517508, at *3 (D. Del. Mar. 31, 2015) ("The fact that the '123 patent was referenced during prosecution of two of defendant's over 1,700 patents … is not compelling evidence of knowledge …."). Therefore, based on the undisputed lack of pre-suit knowledge of the asserted patents, the Court should, at minimum, grant summary judgment of no willful infringement and no indirect infringement for the pre-suit period.

The Court should also grant summary judgment of no willful infringement and no indirect infringement for the post-suit period because the Court should not allow VLSI to rely on the complaint as providing Intel with the requisite knowledge of the patents—particularly where it sued Intel without any prior outreach. *See Sonos*, 591 F. Supp. 3d at 648 ("[W]ithout a notice letter or circumstances like the examples described previously, the complaint will generally not be adequate to serve as notice for either willful or indirect infringement."); *Splunk Inc. v. Cribl, Inc.*, No. C22-07611 WHA, 2023 WL 2562875, at *2-4 (N.D. Cal. Mar. 17, 2023) (similar); *ZapFraud, Inc. v. Barracuda Networks, Inc.*, 528 F. Supp. 3d 247, 250 (D. Del. 2021) ("[T]he complaint itself cannot be the source of the knowledge required to sustain claims of induced infringement and willfulness-based enhanced damages.").[6]

[6] Although some courts have found that a complaint can provide adequate notice of patents, this Court should decline to do so here because VLSI should not be permitted to "create" its willful and indirect infringement claims "by filing claims." *See ZapFraud*, 528 F. Supp. 3d at 251. In any event, there is

Second, lacking sufficient evidence that Intel even knew of the asserted patents—much less their contents—the undisputed facts also demonstrate that Intel did not have the requisite "knowledge of infringement." *Dali*, 2022 WL 16701926, at *5. That is especially the case here where VLSI alleges "no more than ordinary infringement" since it filed the complaint. *Droplets, Inc. v. Yahoo! Inc.*, No. 12-cv-03733-JST, 2021 WL 9038501, at *13 (N.D. Cal. July 2, 2021) (granting summary judgment of no willful infringement); *see also Bayer Healthcare LLC v. Baxalta Inc.*, 989 F.3d 964, 988 (Fed. Cir. 2021) (affirming JMOL of no willful infringement where "evidence adduced at trial merely demonstrates [defendant's] knowledge of the … patent and … direct infringement of the asserted claims"); *Cyph, Inc. v. Zoom Video Commc'ns, Inc.*, No. 22-cv-00561-JSW, 2022 WL 17170146, at *9 (N.D. Cal. Nov. 22, 2022) (dismissing claim for willful infringement based on allegation of continued infringement after filing of complaint); *Google LLC v. Princeps Interface Techs. LLC*, No. 19-cv-06566-EMC, 2020 WL 1478352, at *2-6 (N.D. Cal. Mar. 26, 2020) (dismissing claims for willful and indirect infringement where patentee "allege[d] no particular facts establishing egregious conduct," "made insufficient allegations of specific intent," and failed to allege that defendant "knew its products were not … capable of substantial non-infringing use"). Moreover, every Intel witness questioned on the subject testified that they were unaware of the asserted patents before this case and that Intel does not infringe. Ex. 40 [Schrom Dep.] 32:19-34:1, 62:12-16, 68:23-69:6, 76:16-79:2, 89:1-90:16, 119:23-120:3, 132:13-24, 138:7-139:4, 141:5-146:3, 151:10-152:6, 156:1-157:23, 158:24-159:18, 162:5-16, 163:6-164:24, 175:3-7, 185:9-12; Ex. 41 [Gunther Dep.] 102:25-103:17, 104:8-16, 105:1-107:8; Ex. 42 [Jen Dep.] 13:9-15, 41:17-42:13, 101:20-23; Ex. 43 [Baldwin Dep.] 121:18-22, 141:5-8, 144:1-147:4, 154:2-155:3; Ex. 44 [Ingerly Dep.] 84:8-85:8, 107:11-13, 109:15-112:10, 114:8-16, 116:10-118:2, 121:4-20; Ex. 3 [Ramani Dep.] 169:24-179:11, 184:10-185:11; Ex. 6 [Therien 1/27/23 Dep.] 409:11-419:8; Ex. 4 [McGavock Dep.] 128:2-134:1; Ex. 11 [Cavagnaro Dep.] 172:2-8, 195:22-203:8; Ex. 8 [L. Brown Dep.] 10:12-11:6, 179:16-183:6, 208:25-209:18; Ex. 45 [Shchupak Dep.] 126:22-24, 127:10-131:20; Ex. 12 [Johnson Dep.] 192:25-

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also no dispute of material fact that VLSI cannot meet its burden to show that Intel had actual knowledge of infringement. *Infra* pp. 23-24.

193:5, 193:20-196:17; Ex. 46 [Conary Dep.] 146:22-25, 147:10-149:8; Ex. 47 [Kreitzer Dep.] 39:20-25; Ex. 48 [Brayton Dep.] 34:15-16.

Because the undisputed facts demonstrate that Intel lacked the notice or knowledge required to prove willful and indirect infringement, summary judgment on those claims should be granted. *See Power Integrations, Inc. v. ON Semiconductor Corp.*, 396 F. Supp. 3d 851, 891-92 (N.D. Cal. 2019) (Freeman, J.) (granting summary judgment of no willful infringement where no evidence of pre-suit notice of patents or alleged infringement); *Finjan, Inc. v. Cisco Sys.*, No. 17-cv-00072-BLF, 2017 WL 2462423, at *5 (N.D. Cal. June 7, 2017) (Freeman, J.) (dismissing claim for willful infringement where patentee "failed to make sufficient factual allegations that [defendant] had pre-suit knowledge of the Asserted Patents or that [defendant's] behavior was 'egregious … beyond typical infringement'"); *Sonos*, 591 F. Supp. 3d at 646-49 (dismissing willful and indirect infringement claims where plaintiff provided defendant with copy of complaint one day before filing); *Splunk*, 2023 WL 2562875, at *2-4 (dismissing willful and indirect infringement claims where plaintiff did not provide pre-suit notice).

B. Intel Is Entitled To Summary Judgment Of No Enhanced Damages.

Summary judgment of no enhanced damages should enter, regardless of whether the Court grants summary judgment of no willful infringement. Courts may award enhanced damages only in "egregious cases," and only for "culpable behavior" that is "wanton, malicious, bad-faith, deliberate, consciously wrongful, flagrant, or—indeed—characteristic of a pirate." *Halo Elecs., Inc. v. Pulse Elecs., Inc.*, 579 U.S. 93, 103-04 (2016). VLSI has offered no evidence that Intel's conduct came even remotely close to meeting that heightened standard. *See* Ex. 39 [Interrog. Resp.] 8-10 (failing to identify evidence of "egregious" conduct necessary for enhanced damages); Dkt. 477-3 [VLSI's Fifth Suppl. Damages Contentions] 216-218 (same). To the contrary, the record shows nothing more than a "'garden-variety' hard-fought patent case" in which Intel has advanced non-frivolous defenses. *See Presidio Components, Inc. v. Am. Tech. Ceramics Corp.*, 875 F.3d 1369, 1382-83 (Fed. Cir. 2017) (affirming decision denying enhanced damages); *Finjan*, 2017 WL 2462423, at *5 (finding patentee "failed to allege facts that [] support a plausible inference that [defendant] engaged in 'egregious' conduct that would warrant enhanced damages").

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X. CONCLUSION

For these reasons, Intel's Omnibus Motion for Summary Judgment should be granted.

Respectfully submitted,

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